ORIENTAL®
SEMICONDUCTOR

Digital Dual-Phase Interleaved PFC Controller with I2C & UART Interfaces

HP1011A

FEATURES

- Digital dual-phase interleaved PFC controller with inherent current matching
- High flexibility digital PWM
    - PWM frequency ranges from 20 kHz to 200 kHz
    - Switching frequency spread spectrum for improved EMI
- High performance control loop
    - 25 MHz sigma-delta ADC for line voltage and current sense, 12.5 MHz sigma-delta ADC for output voltage
    - Enhanced dynamic loop response
    - Input voltage feedforward to avoid reverse current during AC drop
    - Control loop parameters can be configured separately for operating modes and input voltage
    - Support HVDC input
- Multi−mode operations
    - Continuous Conduction Mode (CCM) in heavy load Conditions
    - Discontinuous Conduction Mode (DCM) in light load conditions
    - Burst mode in the zero load conditions
    - The mode parameters can be configured separately for high line and low line
- Advanced control functions
    - True RMS power metering
    - Inrush current control with programming relay delay
    - Output voltage follows power variation
    - Relay power-saving mode
    - PFC quick start function
- Extensive fault protections
    - Fast over-voltage protection
    - Bulk under-voltage protection and over-voltage protection
    - External NTC thermal protection
    - Cycle−by−cycle current limit
    - Average switching current protection
- Built-in 128 bytes MTP to store custom configurations
- Low power consumption
- I2C and UART interfaces
- Programming via easy-to-use Graphical User Interface (GUI)
- Available in QFN-24L packages
- -40°C to 125°C operating temperature

APPLICATIONS

Ultra−High Efficiency Power Supplies
LED Lighting
Industrial Power Supplies
Server/Telecom
EV/E-Bike Charger
Supercomputing
Variable-Frequency Drivers (VFD)

GENERAL DESCRIPTION

The HP1011 is a highly flexible digital Power Factor Correction (PFC) controller designed to drive the dual phase interleaved PFC stage.

A rectified diode bridge and dual-phase interleaved boost converter each has a fast-switching leg driven at the PWM switching frequency and a fast-recovery diode make up the dual-phase interleaved PFC. HP1011 supports shut-down one PWM channel under light load condition which can achieve high efficiency at light load.

The HP1011 offers RMS value of input voltage, current, and power. Through the I2C and UART interfaces, this information can be communicated to a microcontroller.

The HP1011 operates from a single 3.3 V supply. The device is available in 4 mm x 4 mm QFN-24L package specified over an ambient temperature range of −40°C to +125°C.

Rev. 1.0

TYPICAL APPLICATION CIRCUIT

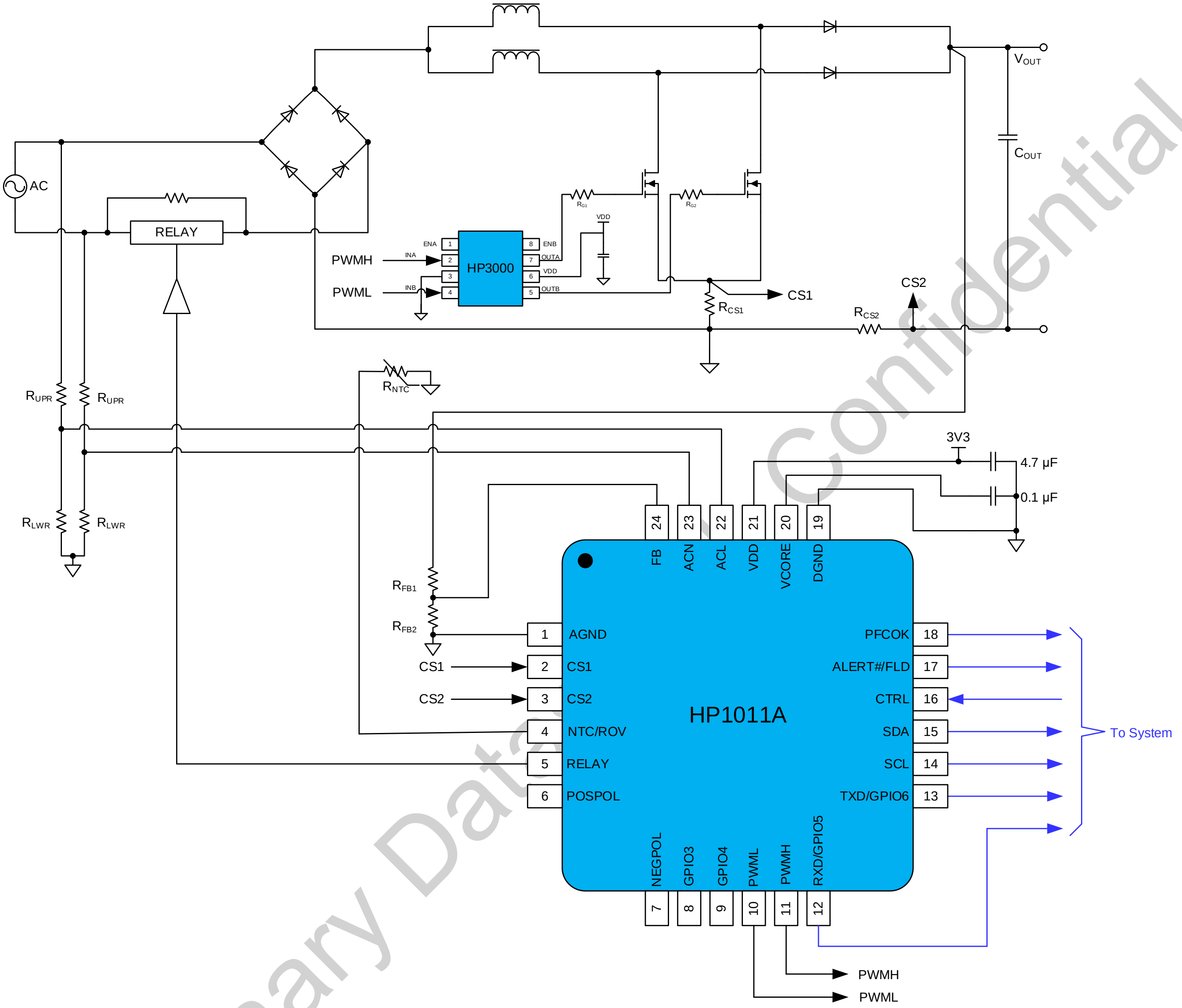

Figure 1 Typical Application Circuit

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

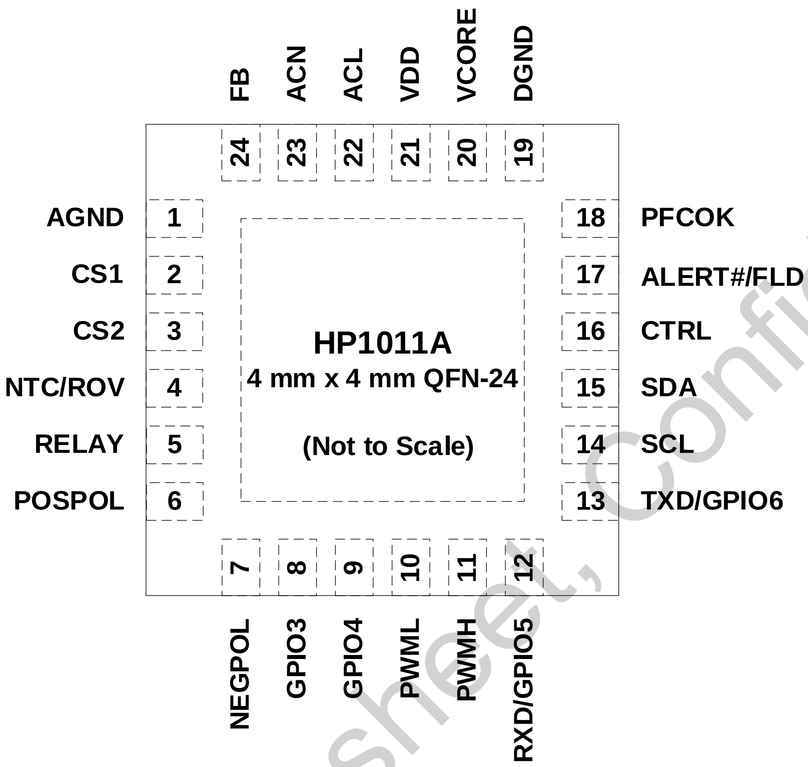


Figure 2 HP1011A-AA000-QN24R Pin Assignment

Table 1. Pin Function Descriptions for HP1011A-AA000-QN24R

Pin No.	Name	Type[1]	Description
1	AGND	P	**Analog ground.** AGND should be connected directly to DGND.
2	CS1	AI	**CS1 Sense.** This pin senses the inductor current upslope through current sense transformers or sense resistor in the DIPFC topology. It is used to reconstruct the inductor current. It is also used for cycle−by−cycle current limiting. The signal is referred to AGND.
3	CS2	AI	**CS2 Sense.** The pin optionally senses the inductor current downslope. The signal is referred to AGND.
4	NTC/ROV	AI	**Dual Function Pin.** NTC: Temperature sense input, which is inverse proportional to the temperature, triggers the comparator when OTP happens. ROV: redundant OVP comparator with a programmable reference. The signal is referred to AGND.
5	RELAY/GPIO0	DO	**Relay Control Output.** The response delay can be programmed. The signal is referred to DGND. It can be re-used as GPIO pin.
6	POSPOL	DO	**Positive Polarity of AC Input.** Positive Output of the internal AC polarity detection circuit. The signal is referred to DGND.
7	NEGPOL	DO	**Negative Polarity of AC Input.** Negative output of the internal AC polarity detection circuit. The signal is referred to DGND.
8	GPIO3	DO	**General-purpose IO.** The signal is referred to AGND.
9	GPIO4	DO	**General-purpose IO.** The signal is referred to AGND.
10	PWML	DO	**PWM logic level output for control of channel 1 switch.** The signal is referred to DGND.

Pin No.	Name	Type[1]	Description
11	PWMH	DO	**PWM logic level output for control of channel 2 switch.** The signal is referred to DGND.
12	RXD/GPIO5	DIO	**UART_RX Pin.** The signal is referred to DGND. It can be re-used as GPIO pin.
13	TXD/GPIO6	DIO	**UART_TX Pin.** The signal is referred to DGND. It can be re-used as GPIO pin.
14	SCL	AIO	**I^{2}C Serial Clock Line.** The SCL signal is referred to DGND.
15	SDA	AIO	**I^{2}C Serial Data Line.** The SDA signal is referred to DGND.
16	CTRL	DI	**Remote Control Pin.** The signal is referred to DGND.
17	ALERT#/FLD	DIO	**I^{2}C Alert Pin.** The signal is referred to DGND. It can be re-used as fast-load transition detection.
18	PFCOK	DIO	**PFCOK Indicates Pin.** The PFCOK function is held low when the PFC output voltage is out of regulation and during fault conditions. It is a push−pull output.
19	DGND	P	**Digital Ground.** DGND should be connected directly to AGND.
20	VCORE	P	**1.8 V VDD for Digital Core.** The VCORE signal is referred to DGND. Connect a 100 nF capacitor from VCORE to DGND.
21	VDD	P	**3.3 V Main Supply.** The VDD signal is referred to AGND. Connect a 4.7 μF capacitor from VDD to AGND.
22	ACL	AI	**AC Line Voltage Sense.** The signal is referred to AGND.
23	ACN	AI	**AC Neutral Voltage Sense.** The signal is referred to AGND.
24	FB	AI	**PFC Output Voltage Sense.** The signal is referred to AGND.

[1] Legend:

A = Analog Pin
P = Power Pin
D = Digital Pin
I = Input Pin
O = Output Pin

SPECIFICATIONS

V_{DD} = 3.0 V to 3.6V, T_J = −40°C to +125°C for minimum and maximum specifications, and T_A = 25 °C for typical specifications, unless otherwise noted.

Table 1. Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
POWER SUPPLY						
Operating Supply Voltage	V_{DD}	4.7 µF capacitor connected to AGND	3	3.3	3.6	V
Supply Current	I_{DD}	Normal operation		10.0		mA
		V_{DD} = 3.3 V while programming			7.5	mA
Shutdown Current	I_{DD_SD}	PFC off state		8.1		mA
Sleep Mode Current	I_{DD_SM}	Sleep mode enabled.		1.0		mA
POWER-ON RESET						
Power-on Reset	V_{DD_POR}	V_{DD} rising	2.7	2.8	2.9	V
UVLO	V_{DD_UVLO}	V_{DD} falling	2.55	2.65	2.75	V
VCORE PIN						
Output Voltage	V_{CORE}	100 nF capacitor connected to DGND	1.7	1.8	1.9	V
OSCILLATOR, CLOCK, PLL						
Oscillator Frequency	f_{OSC}		11.875	12.5	13.125	MHz
PLL Frequency	f_{PLL}		190	200	210	MHz
Digital PWM Resolution	t_{PWM_RES}	For PWML and PWMH pins		5		ns
PWMH, PWML, GPIO3, GPIO4, POSPOL, NEGPOL, RELAY PINS						
Output Low Voltage	V_{PWMOL}	Sink current = 10 mA			0.4	V
Output High Voltage	V_{PWMOH}	Source current = 10 mA	V_{DD}-0.4			V
Rise time	t_{RISE}	V_{DD} = 3.3 V , C_{LOAD} = 50pF 10%V_{DD} to 90%V_{DD}		25		ns
Fall time	t_{FALL}	V_{DD} = 3.3 V , C_{LOAD} = 50 pF 90% V_{DD} to 10%V_{DD}		25		ns
Output Source Current	I_{OL}	V_{DD} = 3.3 V	-10			mA
Output Sink Current	I_{OH}	V_{DD} = 3.3 V			10	mA
SWITCHING FREQUENCY						
Frequency Range	f_{SW}		20		195	kHz
Accuracy			-3%		3%	
ACN AND ACL PINS						
Input Impedance				78		kΩ
Input Voltage Range	V_{AC}		0		2.8	V
Amplifier Gain	G_{AC_OP}			0.5		
ADC						
ADC range			0		1.4	V
ADC Clock Frequency				25		MHz
Equivalent Resolution		Data updating frequency 25 kHz		10		Bits
Voltage Sense Accuracy		20% to 90% of usable range -40°C < T_A < 125°C	-2.0		2.0	%

Parameter	Symbol	Conditions	Min	Typ	Max	Units
AUX Positive Comparator						
Threshold Range 错误!未定义书签。			40		340	mV
Threshold Accuracy		Test at 200mV Threshold	-30		30	
Resolution				4		Bit
LSB				20		mV
Hysteresis				40		mV
Propagation Delay					1.0	µs
AUX Negative Comparator						
Threshold Range 错误!未定义书签。			40		340	mV
Threshold Accuracy		Test at 200mV Threshold	-30		30	
Resolution				4		Bit
LSB				20		mV
Hysteresis				40		mV
Propagation Delay					1.0	µs
AC Line Frequency Monitor						
High Threshold	f_{5060_H}		68	70	72	Hz
Lower Threshold	f_{5060_L}		37	40	43	Hz
Detection Timer	N_{LINE_DET}		0.5		2	cycles
Exceed Timer	$N_{LINE\_FREQ\_EXC}$			2		cycles
Brown-out and SAG						
Vin On Threshold	V_{IN_ON}	Programmable, $K_{AC\_DIV\_EXT}$=1/200	0	78	255	VAC
Vin Off Threshold	V_{IN_OFF}	Programmable, $K_{AC\_DIV\_EXT}$=1/200	0	71	255	VAC
Brown-out Debounce	t_{BO_DEB}		-	0.5	-	cycles
Line Sag Timeout Range	t_{SAG_TO}	Programmable 4 to 32 AC cycles	4	12	32	cycles
High/Low Line Detection						
High Threshold	V_{HLINE}	Programmable, $K_{AC\_DIV\_EXT}$=1/200	120	168	180	VAC
Low Threshold	V_{LLINE}	Programmable, $K_{AC\_DIV\_EXT}$=1/200	120	156	180	VAC
High Line to Low Line Debounce Time	t_{H2L_DED}			1		cycles
VAC ZERO CROSSING DETECTION						
VAC Zero Detection Comparator		Between ACL Pin to ACN pin				
Threshold	V_{POL_DET}		-10	0	10	mV
Hysteresis Width	V_{POL_HYS}			10		mV
Propagation Delay	t_{POL_PD}				1.0	µs
Digital Polarity Detection						
Digital Propagation Delay				5		µs
VIN_POL Detection Debounce	t_{POL_DEB}		5		80	µs
VIN_POL Detection LSB				5		µs
FB PIN						
Input Voltage			0		2.8	V

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Impedance				350		kΩ
Amplifier Gain				0.5		
ADC						
ADC Range			0		1.4	V
ADC Clock Frequency				12.5		MHz
Equivalent Resolution				11		Bits
Voltage Sense Accuracy		20% to 90% of usable range -40°C < T_A < 125°C	-1		1	%
Fast Over-Voltage Protection						
Threshold Range	$V_{FB\_FOV\_LIM}$		1.9		2.5	V
Threshold Accuracy		Factory trimmed at 2.2 V	-1.5		1.5	%
Resolution				6		Bits
Hysteresis				100		mV
Propagation Delay	$t_{FB\_FOV\_PD}$				160	ns
Debounce Time	$t_{FB\_FOV\_DB}$	Programmable in 4 steps	40		100	µs
Blanking time	$t_{FB\_FOV\_BK}$			10		µs
Open Loop Protection						
Sink Current	I_{FB_SNK}			250		nA
Threshold	V_{FB_OL}		2		70	V
Resolution				4		Bits
Hysteresis	V_{FB_OLHYS}			18		V
Debounce Time	t_{FB_OLDB}	Programmable in 4 steps	1		4	cycles
Slow Over-Voltage Protection						
Threshold	$V_{FB\_SOV\_LIM}$		V_{REF}		V_{REF}+68	V
Resolution				5		Bits
Accuracy			-2		+2	%
Debounce Time	$t_{FB\_SOV\_DB}$		0		0.48	ms
Slow Under-Voltage Protection						
Threshold			V_{REF}-68		V_{REF}	V
Resolution	$V_{FB\_SUV\_LIM}$			5		Bits
Accuracy			-2		+2	%
Debounce Time	$t_{FB\_SUV\_DB}$		0		30	ms
CS1 AND CS2 PINS						
Input Voltage			0		1.4	V
Input Impedance				160		kΩ
Amplifier Gain				1		
ADC						
ADC Range			0		1.4	V
ADC Clock Frequency				25		MHz
Equivalent Resolution		Updating frequency at 100 kHz		8		Bits
Current Sense Accuracy		20% to 90% of usable range -40°C < T_A < 125°C	-1.5		1.5	%
CS1 Fast Over Current Protection						
Threshold Range	$V_{CS1\_OC\_LIM}$		1.0		1.5	V

Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
Threshold Accuracy		Factory trimmed at 1.25 V	-1.2		0.48	%
Resolution				6		Bits
LSB				7.8		mV
Hysteresis				25		mV
Propagation Delay					100	ns
Blanking Time		Programmable in 4 steps	480		1920	ns
Debounce Time		Programmable in 4 steps	80		200	ns
CTRL PIN						
Input High Voltage	V_{CTRL_IL}				0.8	V
Input Low Voltage	V_{CTRL_IH}		2.0			V
Debounce Time	t_{CTRL_DEB}			10		µs
Leakage Current	i_{CTRL_LK}				1.0	µA
PFCOK PINS						
Output Low Level					0.8	V
Output High Level			2.0			V
Debounce Time			0		200	ms
OVER AVERAGE SWITCHING CURRENT PROTECTION						
Average OCP Threshold		CS1 Sense ratio is 10:1	0		14	A
Resolution				7		Bits
Accuracy			-2		+2	%
Debounce				2		Switch cycle
NTC/ROV PIN						
Current Source	I_{NTC}		43	46	49	µA
Over-temperature Threshold	V_{NTC_OT}		0.36	0.4	0.41	V
OT Recover Threshold	V_{NTC_REC}		0.78	0.8	0.82	V
Debounce Time	t_{NTC_DEB}	Programmable in 2 steps		500	1000	ms
Redundant Over-Voltage Protection						
Threshold Range	V_{ROV_LIM}		1.9	2.2	2.5	V
Threshold Accuracy		Factory trimmed at 2.2 V	-2.00		1.64	%
Resolution				6		Bits
Hysteresis				100		mV
Propagation Delay					160	ns
Debouncing Time		Programmable in 4 steps	40		100	µs
Blanking Time				10		µs
SDA/SCL PINS						
Input Voltage Low					0.8	V
Input Voltage High			2.2			V
Output Voltage Low					0.4	V
Pull-Up Current			100		350	µA
Leakage Current			−5		+5	µA
SERIAL BUS TIMING						

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Clock Frequency	f_{IIC}				400	kHz
Glitch Immunity	t_{SW}				50	ns
Bus Free Time	t_{BUF}		4.7			µs
Start Setup Time	t_{SU_STA}		4.7			µs
Start Hold Time	t_{HD_STA}		4			µs
SCL Low Time	t_{LOW}		4.7			µs
SCL High Time	t_{HIGH}		4			µs
SCL, SDA Rise Time	t_{R_I2C}				1000	ns
SCL, SDA Fall Time	t_{F_I2C}				300	ns
Data Setup Time	t_{SU_DAT}		250			ns
Data Hold Time	t_{HD_DAT}		300			ns
TXD/RXD PINS (UART)						
Baud Rate	f_{UART}	Programmable with (0:9600; 1: 1200; 2: 57600; 3: 115200)	1200	9600	115200	bps
Data Length				8		
Stop Bits				1		
Polarity Check Bit				1		
EEPROM RELIABILITY						
Endurance		T_A = 85°C	10,000			Cycles
		T_A = 125°C	1000			Cycles
Data Retention		T_A = 85°C	20			Years
		T_A = 125°C	15			Years

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute maximum ratings

Parameter	Rating
VDD (Continuous)	4.2 V
ACL, ACN, FB, CS1, CS2, RELAY, NTC/ROV, POSPOL, NEGPOL, GPIO3, GPIO4, PWML, PWMH, RXD/GPIO5, TXD/GPIO6, SCL, SDA, CTRL, ALERT#/FLD ,PFCOK	-0.3 V to V_{DD} + 0.3 V
VCORE	2 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Maximum Junction Temperature	150°C
Soldering Conditions	JEDEC J-STD-020
Electrostatic Discharge (ESD)	
Human Body Model	±6000 V
Charge Device Model	±2000 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
QFN4x4-24L	46	23	°C/W

ESD CAUTION

	**Electrostatic Discharge Sensitive Device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

APPLICATION INFORMATION

DUAL-PHASE INTERLEAVED PFC

Dual-phase interleaved PFC typical application circuit is shown in Figure 3.

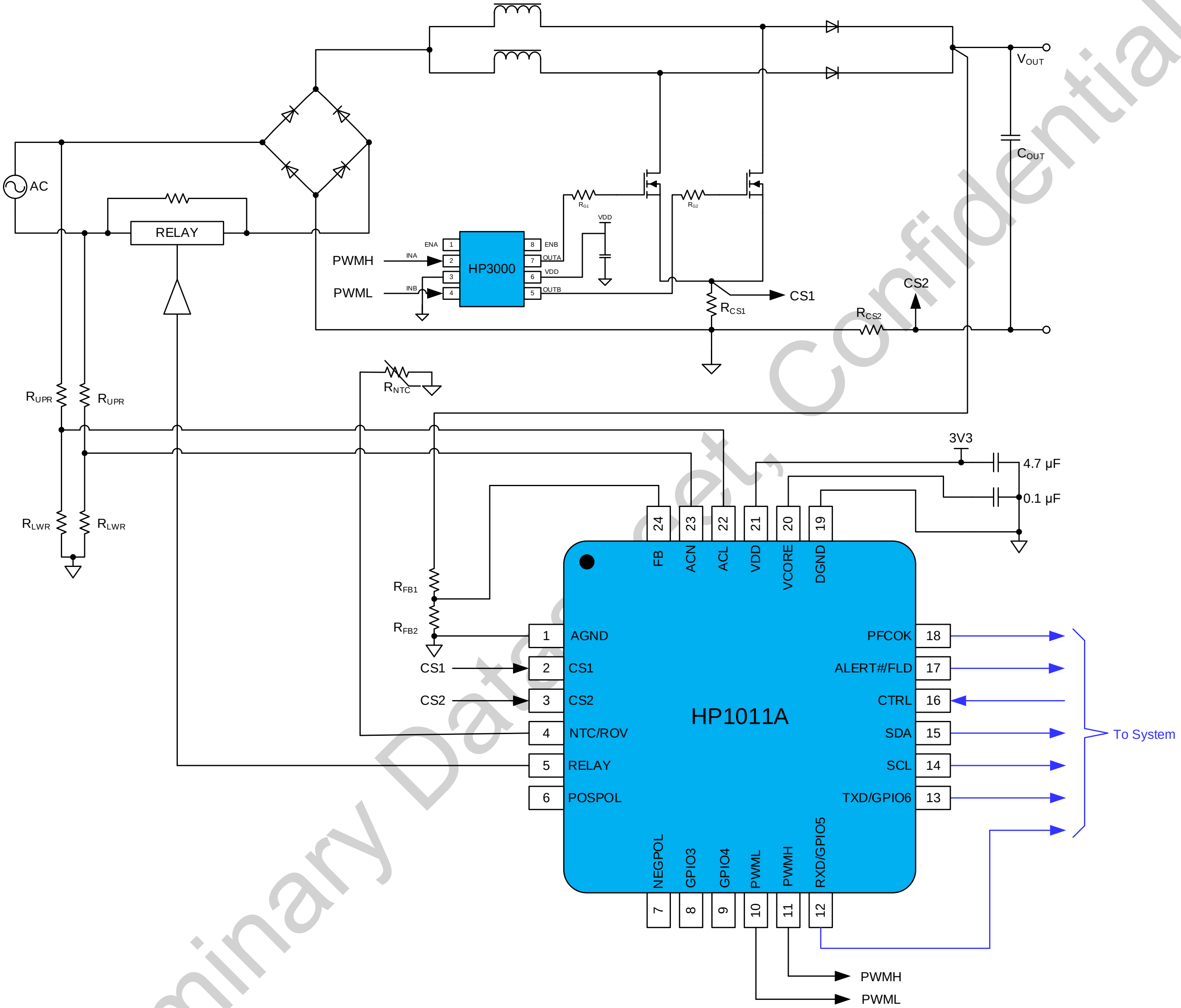
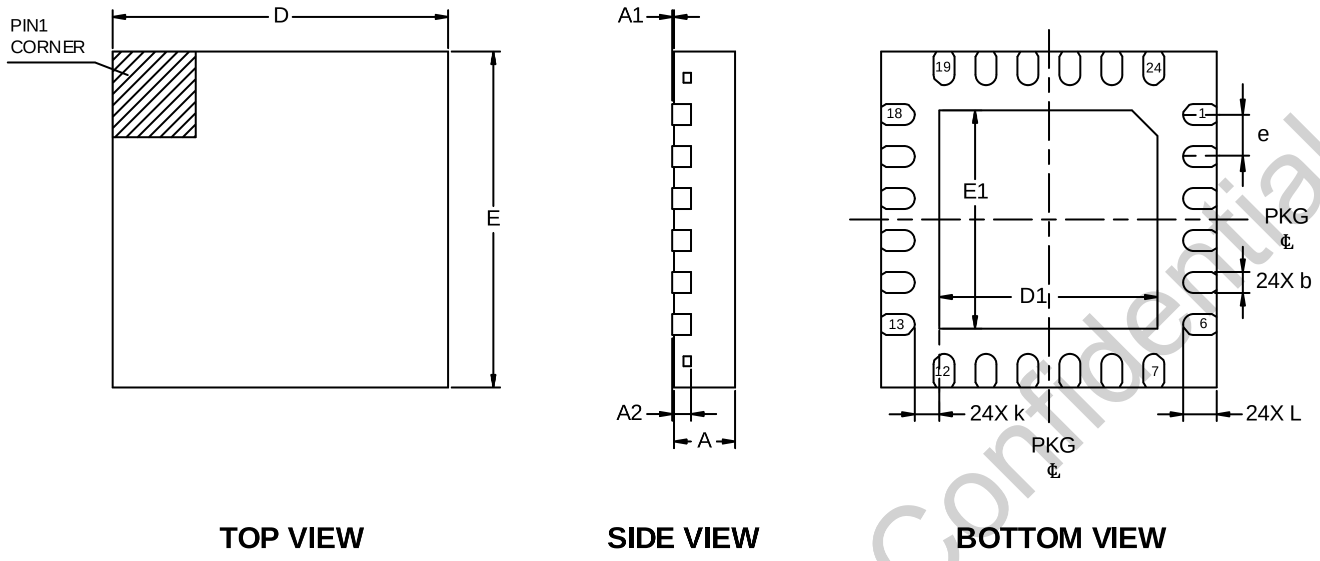


Figure 3 Dual-phase Interleaved PFC Typical Application Circuit

PACKAGE OUTLINE DIMENSIONS



SYMBOLS	DIMENSION IN MILLIMETERS		
	MIN	**NOM**	**MAX**
A	0.70	0.75	0.80
A1	0.000	0.02	0.05
A2	0.203 REF		
b	0.18	0.25	0.30
D	4.00 BSC		
E	4.00 BSC		
D1	2.40	2.70	2.80
E1	2.40	2.70	2.80
e	0.50 BSC		
L	0.30	0.40	0.50
k	0.20 MIN		

Figure 4 HP1011A-AA000-QN24R Dimension

PACKAGE TOP MARKING

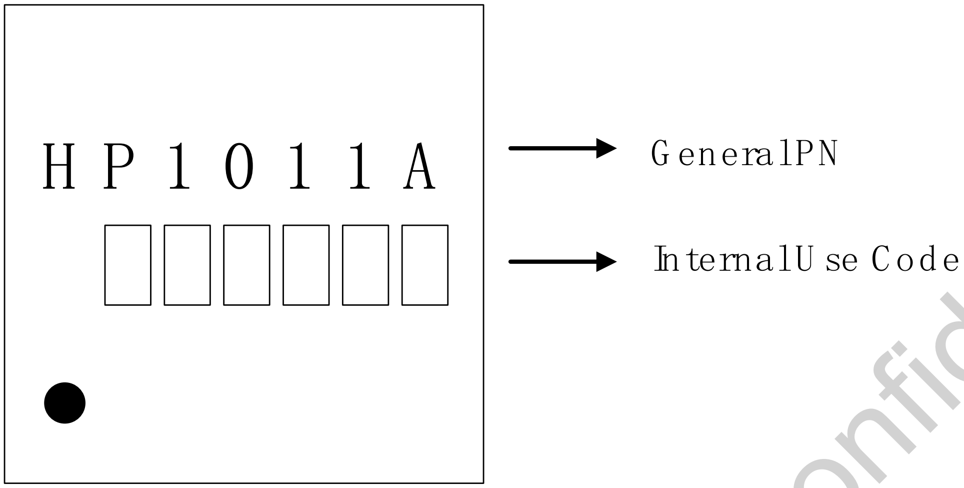


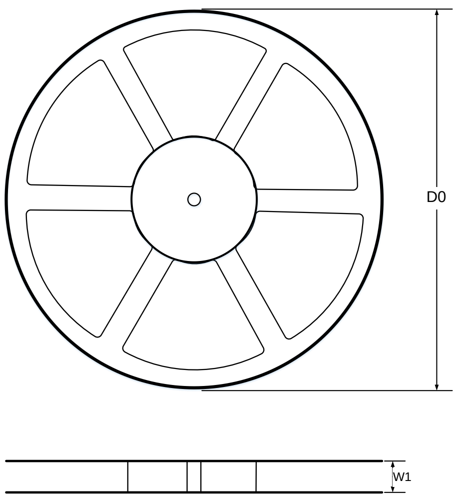
Figure 5 HP1011A-AA000-QN24R Package Top Marking

ORDERING GUIDE

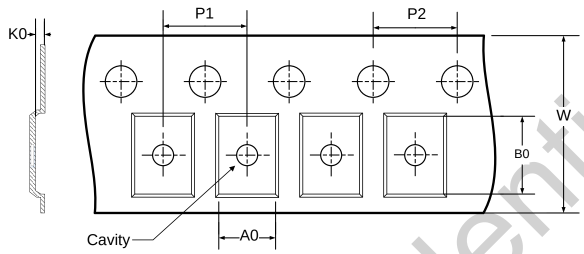
Model	Temperature Range	Package Type	MSL	Package Option	Quantity
HP1011A-AA000-QN24R	-40°C to +125°C	QFN4x4-24L	3	T&R	5000

TAPE AND REEL INFORMATION

REEL DIMENSIONS

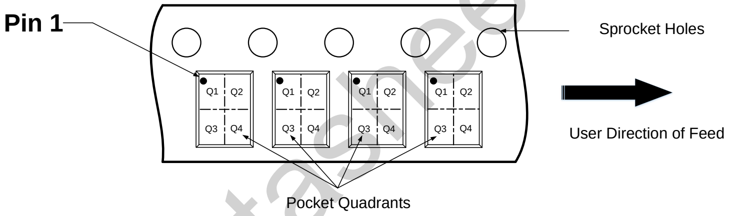


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D0：Reel Diameter
W1：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



DIMENSIONS AND PIN1 ORIENTATION

Device	Package Type	D0 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant	Quantity
HP1011A-AAXXX-QN24R	QFN4X4-24L	330.00	12.40	4.30	4.30	1.10	8.00	4.00	12.00	Q1	5000

All dimensions are nominal

Figure 6 Tape and Reel Information

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